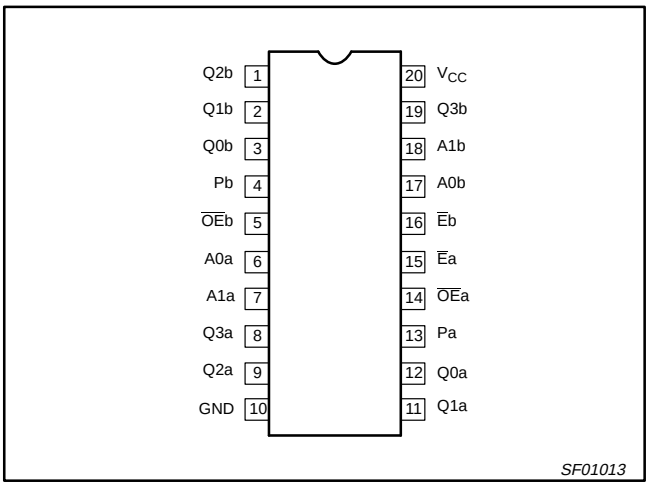
Dual 1-of-4 decoder (3-State) 74F539

DESCRIPTION

The 74F539 contains two independent decoders. Each accepts two address (A0 - A1) input signals and decodes them to select one of four mutually exclusive outputs. A Polarity control (P) input determines whether the outputs are active Low (P=H) or active High (P=L). An active-Low Enable ($\overline{E}$) is available for data demultiplexing. Data is routed to the selected output in non-inverted or inverted form in the active-Low mode or inverted form in the active-High mode. A High signal on the Output Enable ($\overline{OE}$n) input forces the 3-State outputs to the high impedance state.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F539	7.5ns	40mA

PIN CONFIGURATION



ORDERING INFORMATION

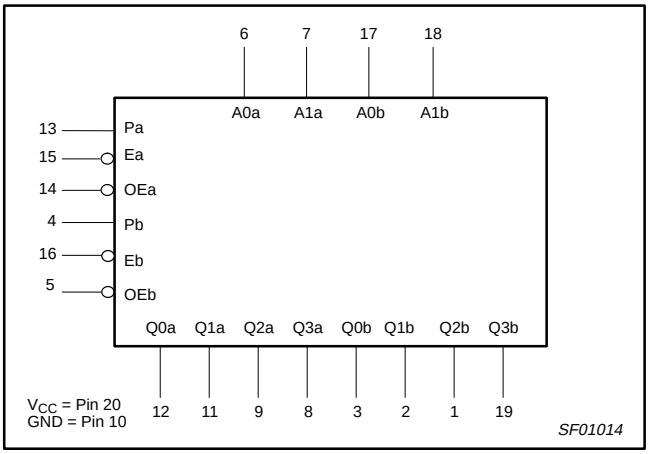
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
20-Pin Plastic DIP	N74F539N
20-Pin Plastic SOL	N74F539D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

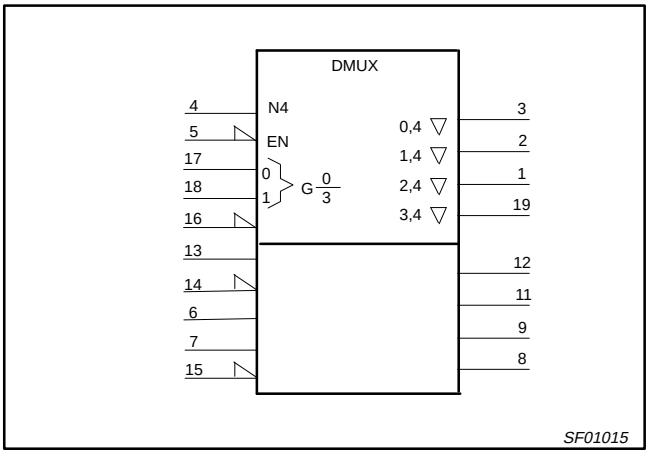
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0a - A1a	Decoder A Address inputs	1.0/1.0	20µA/0.6mA
A0b - A1b	Decoder B Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}$a, $\overline{E}$b	Enable inputs (active Low)	1.0/1.0	20µA/0.6mA
$\overline{OE}$a, $\overline{OE}$b	Output Enable inputs (active Low)	1.0/1.0	20µA/0.6mA
Pa, Pb	Polarity control inputs	1.0/1.0	20µA/0.6mA
Q0a–Q3a	Decoder A Data outputs	150/40	3.0mA/24mA
Q0b–Q3b	Decoder A Data outputs	150/40	3.0mA/24mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

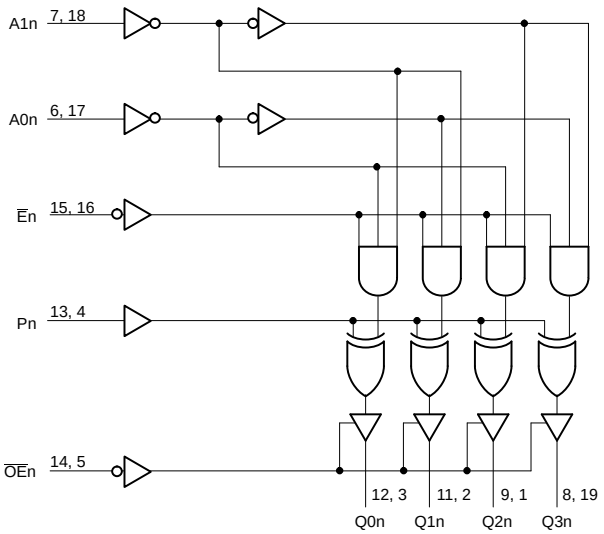
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10

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FUNCTION TABLE

INPUTS				OUTPUTS				OPERATING MODE
$\overline{OE}_n$	$\overline{E}$n	A1n	A0n	Q0n	Q1n	Q2n	Q3n	
H	X	X	X	Z	Z	Z	Z	High Impedance
L	H	X	X	Qn=P				Disable
L	L	L	L	H	L	L	L	Active High output (P = L)
L	L	L	H	L	H	L	L	
L	L	H	L	L	L	H	L	
L	L	H	H	L	L	L	H	
L	L	L	L	L	H	H	H	Active Low output (P = H)
L	L	L	H	H	L	H	H	
L	L	H	L	H	H	L	H	
L	L	H	H	H	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–3	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.4			V
			±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
			±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OZH}	Off-state output current High-level voltage applied	V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current Low-level voltage applied	V_{CC} = MAX, V_O = 0.5V				–50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current	I_{CCH}	V_{CC} = MAX		35	50	mA
		I_{CCL}			40	55	mA
		I_{CCZ}			40	60	mA

NOTES:

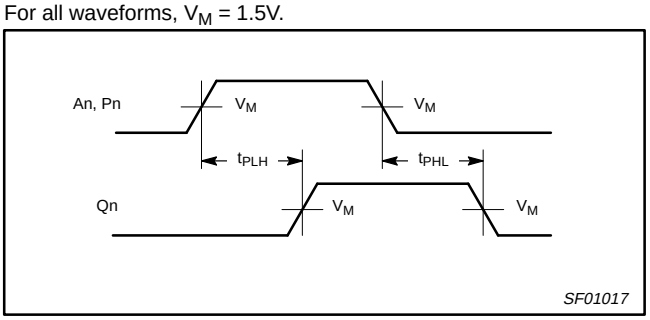
1. For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

AC ELECTRICAL CHARACTERISTICS

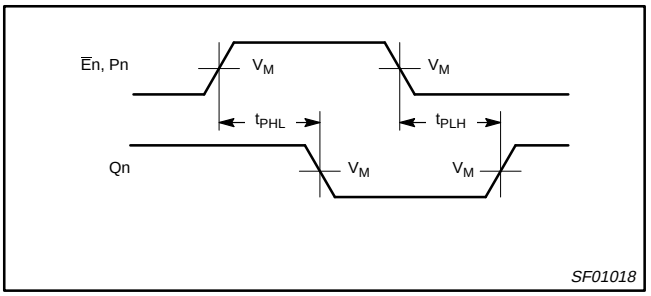
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Qn	Waveform 1	4.5 3.0	8.5 8.0	12.5 12.5	4.0 3.0	13.5 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$n to Qn	Waveform 2	5.0 3.0	7.5 7.0	11.0 11.0	4.5 3.0	12.0 11.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Pn to Qn	Waveform 1	4.0 3.5	6.5 5.5	9.5 9.0	3.5 3.0	10.5 9.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Pn to Qn (INV)	Waveform 2	6.0 4.0	11.5 6.0	14.5 9.0	5.0 4.0	15.5 9.5	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$n to Qn	Waveform 3 Waveform 4	2.5 5.5	4.0 7.0	7.5 10.5	2.0 5.0	8.5 11.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$n to Qn	Waveform 3 Waveform 4	1.5 2.0	3.0 4.0	6.0 8.0	1.0 1.5	6.5 8.5	ns ns

AC WAVEFORMS

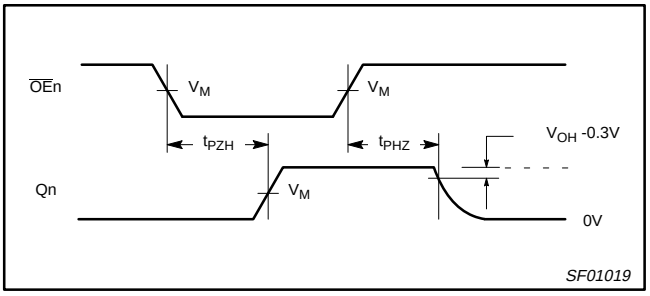
For all waveforms, V_M = 1.5V.



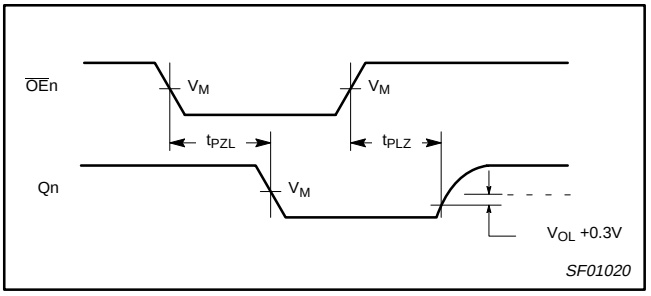
Waveform 1. Propagation Delay for Non-Inverting Outputs



Waveform 2. Propagation Delay for Inverting Outputs

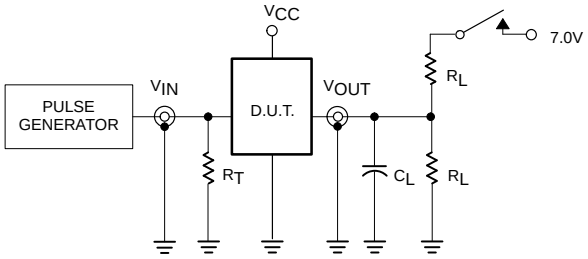


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

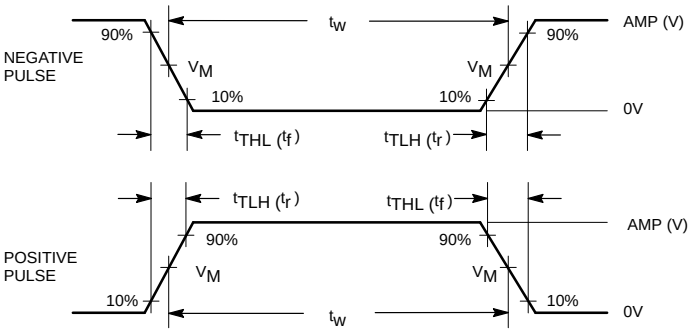


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

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